LEADLESS PLASTIC CHIP CARRIER WITH ETCH BACK PAD SINGULATION

Cross-Reference to Related application

This is a continuation-in-part of U.S. patent application serial no. 09/288,352, filed April 8, 1999, which is a continuation-in-part of U.S. patent application serial no. 09/095,803, filed June 10, 1998.

Field of the Invention

The present invention relates in general to integrated circuit packaging, and more particularly to an improved process for fabricating a leadless plastic chip carrier which includes a post mold etch back step and unique contact pad and die attach pad design features.

Background of the Invention

According to well known prior art IC (integrated circuit) packaging methodologies, semiconductor dice are singulated and mounted using epoxy or other conventional means onto respective die pads (attach paddles) of a leadframe strip. Traditional QFP (Quad Flat Pack) packages incorporate inner leads which function as lands for wire bonding the semiconductor die bond pads. These inner leads typically require mold locking features to ensure proper positioning of the leadframe strip during subsequent molding to encapsulate the package. The inner leads terminate in outer leads that are bent down to contact a mother board, thereby limiting the packaging density of such prior art devices.

In order to overcome these and other disadvantages of the prior art, the Applicants previously developed a Leadless Plastic Chip Carrier (LPCC). According to Applicants' LPCC methodology, a leadframe strip is provided for supporting up to several hundred devices. Singulated IC dice are placed on the strip die attach pads

using conventional die mount and epoxy techniques. After curing of the epoxy, the dice are gold wire bonded to peripheral internal leads. The leadframe strip is then molded in plastic or resin using a modified mold wherein the bottom cavity is a flat plate. In the resulting molded package, the die pad and leadframe inner leads are exposed. By exposing the bottom of the die attach pad, mold delamination at the bottom of the die paddle is eliminated, thereby increasing the moisture sensitivity performance. Also, thermal performance of the IC package is improved by providing a direct thermal path from the exposed die attach pad to the motherboard. By exposing the leadframe inner leads, the requirement for mold locking features is eliminated and no external lead standoff is necessary, thereby increasing device density and reducing package thickness over prior art methodologies. The exposed inner leadframe leads function as solder pads for motherboard assembly such that less gold wire bonding is required as compared to prior art methodologies, thereby improving electrical performance in terms of board level parasitics and enhancing package design flexibility over prior art packages (i.e. custom trim tools and form tools are not required). These and several other advantages of Applicants' own prior art LPCC process are discussed in Applicants' co-pending patent application serial no. 09/095,803, the contents of which are incorporated herein by reference.

Applicants' LPCC production methodology utilizes saw singulation to isolate the perimeter I/O row as well as multi-row partial lead isolation. Specifically, the leadframe strip is mounted to a wafer saw ring using adhesive tape and saw-singulated using a conventional wafer saw. The singulation is guided by a pattern of fiducial marks on the bottom side of the leadframe strip. Also, special mold processing techniques are used to prevent the mold flow from bleeding onto the functional pad area and inhibiting electrical contact. Specifically, the exposed die pad surface is required to be deflashed after molding to remove any molding compound residue and thereby allow the exposed leads and die attach pad to serve as solder pads for attachment to the motherboard.

According to Applicant's co-pending U.S. patent application serial no. 09/288,352, the contents of which are incorporated herein by reference, an etch back

process is provided for the improved manufacture of the LPCC IC package. The leadframe strip is first subjected to a partial etch on one or both of the top and bottom surfaces in order to create a pattern of contact leads (pads) and a die attach pad (paddle). After wire bonding the contacts to a singulated semiconductor die, followed by overmolding and curing of the mold, the leadframe strip is exposed to a second full etch immersion for exposing the contact pads in an array pattern (i.e. multi-row) or perimeter pattern (i.e. single row), as well as the die attach pad. In the case of a package with multi-row I/O leads, this etch back step eliminates the requirement for two additional saw singulation operations (i.e. to sever the inner leads from the outer leads), and in both the single-row and multi-row configurations, the etch back step eliminates post mold processing steps (e.g. mold deflashing) and ensures superior device yield over the processing technique set forth in Applicants' prior application no. 09/095,803. Additionally, using this technique allows for higher I/O pad density and also allows for pad standoff from the package bottom which reduces stress in the solder joint during PCB temp cycling. Further, the technique allows for the use of a pre-singulation strip testing technique given that the electrical I/O pads are now isolated from each other and testing in strip can take place. This feature greatly increased the handling and throughput of the test operation.

Other prior art references teach the concepts of etching back a sacrificial substrate layer to expose contact pads and die attach paddle, such as U.S. Patents 4,530,152 (Roche et al); 5,976,912 (Fukutomi, et al); 6,001,671 (Fjelstad) and Japanese patent application no. 59-208756 (Akiyama).

Summary of the Invention

According to the present invention, Applicant's etch-back LPCC process has been modified to provide additional design features. Firstly, an etch barrier is provided as the first layer of the contact pads and die attach pad, and the contact pads are formed to a "rivet" head shape for improved interlocking and the die attach pad is formed with an interlock pattern for improved alignment with the semiconductor die. Improved electrical performance is enjoyed over the above discussed prior art designs

by incorporation of a ground ring on the die attach pad to which multiple ground pads on the die are parallel bonded. The incorporation of a ground ring on the die attach pad provides a constant distance between the ground ring and the ground pads to which the ground ring is wire bonded. The ground ring is then bonded out to only one of the external I/O pads.

According to a further embodiment of the invention, two concentric rings are provided to allow for both power and ground using only a single I/O pad for each.

According to an additional embodiment, an etch down cavity is provided for solder ball attachment.

Brief Description of the Drawings

A detailed description of the invention is provided herein below with reference to the following drawings, in which:

Figures 1A – 1I show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with top and bottom partial etch resulting in a bottom etch cavity, according to a first embodiment of Applicants' prior art process;

Figures 2A – 2G show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with top and bottom partial etch incorporating standoff, according to a second embodiment of Applicants' prior art process;

Figures 3A – 3H show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with top side partial etch and solder ball attachment, according to a third embodiment of Applicants' prior art process;

Figures 4A – 4I show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with top side partial etch incorporating standoff, according to a fourth embodiment of Applicants' prior art process;

Figures 5A – 5J show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with bottom side partial etch, according to a fifth embodiment of Applicants' prior art process;

Figures 6A – 6H show processing steps for manufacturing a Leadless Plastic Chip Carrier (LPCC) with etch back and special attachment features, according to the present invention;

Figure 7 is a bottom plan view of a single row IC package manufactured in accordance with the process of Figures 6A – 6H; and

Figures 8A and 8B are bottom plan views of array type IC packages manufactured in accordance with the process of Figures 6A – 6H.

Figure 9 is a bottom plan view of an array type IC package according to the present invention, showing a pair of concentric rings.

Detailed Description of Preferred Embodiment

Applicants' prior Leadless Plastic Chip Carrier with Etch Back Singulation (LPCCEBS) process as described in copending application serial no. 09/288,352 is an improvement over Applicants' LPCC process as set forth in co-pending application serial no. 09/095,803. The present invention relates to an improvement in Applicants' prior LPCC methodology. Before describing details of the improvement according to the present invention, reference will be made to Figures 1 to 5 which set forth Applicants' LPCCEBS process. Where possible, the same reference numerals have been used in this application to denote identical features described in Applicants' earlier applications. Reference may be had to Applicants' co-pending applications for additional details concerning processing steps which are common to Applicants' processes.

Figures 1A – 1I show steps in the manufacture of an LPCCEBS according to a first embodiment of the invention disclosed in copending application serial no. 09/288,352 – namely, with top and bottom side partial etch and bottom etch cavity.

With reference to Figure 1A, an elevation view is provided of a copper panel substrate which forms the raw material of the leadframe strip 100. As discussed in greater detail in Applicants' co-pending application serial no. 09/095,803, the leadframe strip 100 is divided into a plurality of sections, each of which incorporates a plurality of leadframe units in an array (e.g. 3 x 3 array, 5 x 5 array, etc.). Only one such unit is depicted in the elevation view of Figure 1A, portions of adjacent units being shown by stippled lines.

The leadframe strip 100 is subjected to a partial etch on both top and bottom sides (Figure 1B) to pattern the contact pads 203 and die attach pad 202. Next, the strip 100 is plated with silver (Ag) or nickel/palladium (Ni/Pd) to facilitate wire bonding (Figure 1C).

A singulated semiconductor die 206 is conventionally mounted via epoxy (or other means) to the die attach pad 202, and the epoxy is cured. Gold wires 205 are then bonded between the semiconductor die 206 and peripheral leads or contacts 203. The leadframe 100 is then molded using a modified mold with the bottom cavity being a flat plate, and subsequently cured, as discussed in Applicants' application serial no. 09/095,803. The leadframe 100 after the foregoing steps is as shown in Figure 1D, which includes overmold 401 of cured plastic or epoxy.

Next, rather than post-mold deflashing, as performed according to Applicants' prior methodology, a wet film layer of photoresist 402 is printed onto the bottom of leadframe 100 so as to cover portions of the bottom surface which are to be protected from etchant (i.e. positive photoresist). The photoresist is then developed (cured) using conventional means (Figure 1E).

The leadframe 100 is then subjected to a final etching via full immersion (Figure 1F) which exposes an array or perimeter pattern of exposed contact pads 203 and the die attach pad 206.

The photoresist layer 402 is then stripped using conventional means (Figure 1G), resulting in small protrusions below the molded body for contact pads 203. After this etch back step, the leadframe strip 100 is coated with either electroless gold or solder dip to facilitate pad soldering (Figure 1H). Alternatively, barrel plated solder or chemically passivated bare copper may be used for terminal finishing.

At this stage of manufacture, the pads 203 and 202 are fully isolated and exposed. Singulation of the individual units from the full leadframe array strip 100 may then be performed either by saw singulation or die punching (Figure 1I).

The embodiment of Figures 2A – 2G is similar to that of Figures 1A – 1I, except that the partial etch (Figure 2B) is a "mirror image" partial etch which results in a "standoff" structure, rather than being an offset pattern as shown in Figure 1B. Consequently, no photoresist application is required following the mold step (Figure 2D) and prior to the final etch back step (Figure 2E).

Applicants' LPCC fabrication process may alternatively utilize a single side first partial etch, as shown in Figures 3 and 4. Figures 3A – 3H show a single side partial etch process wherein, after the final full immersion etch and electroless gold plating (Figures 3E and 3F), the pads 203 are above the mold line so that solder balls 203A are required to be attached in order to allow board mounting. Figures 4A – 4I show a single side first partial etch with standoff (similar in this respect to the process of Figure 2). A layer of photoresist 402 is applied (Figure 4E) and patterned, prior to the final etch back step (Figure 4F). In other respects, the steps depicted in Figures 3 and 4 are similar to the steps discussed above and illustrated in Figures 1 and 2, respectively.

Figures 5A – 5J show steps according to the etch back process of Applicants' prior invention, for fabricating an LPCC with multi-row partial lead isolation. In Figure 5A, a copper panel is provided, to which photoresist 502 is applied and patterned for a "first level" connect (Figure 5B). An electrolytic plat of Cu/Ni/Au is applied to portions of the leadframe strip not covered by photoresist (Figure 5C). The photoresist is then stripped (Figure 5D), resulting in the structure of Figure 5D with contact pads 203 and attach pad 202.

A layer of negative photoresist 504 is applied and patterned for a "second level" connect (Figure 5E). A pre-etch step is then performed (Figure 5F) to create contact and attach pad protrusions on the bottom of the structure. The photoresist 504 is then stripped and the structure is cleaned (Figure 5G).

Next, the semiconductor 206 is attached to the pad 202, gold wire bonds 203 are attached to the multi-row leads 203 and the structure is encapsulated as discussed above in mold 401, such that the contact pad and attach pad protrusions remain exposed (Figure 5H). A final etch back is performed (Figure 5I) and the individual units are singulated. It will be noted that the steps in Applicants' prior LPCC process

of saw singulating between the inner and outer rows of leads, is eliminated. Also, as with the embodiments of Figures 1 to 4, post mold deflashing and cleaning has been eliminated.

Having thus described Applicants' prior LPCC and LPCCEBS methodologies, reference will now be made to Figure 6, 7 and 8 showing the improvements which constitute the present invention.

With reference to Figure 6A, an elevation view is provided of a copper panel substrate which forms the raw material of leadframe strip 100 having thickness of approximately 5 mils. As discussed in greater detail in Applicants' co-pending application serial no. 09/095,803, the leadframe strip is divided into a plurality of sections, each of which incorporates a plurality of leadframe units in an array (e.g. 3 x 3 array, 5 x 5 array, etc.). Only one such unit is depicted in the elevation view of Figure 6A, portions of adjacent units being shown by stippled lines.

The leadframe strip 100 is covered with a photoresist mask 102 (Figure 6B) in order to mask predetermined areas from subsequent multiple deposition steps (Figure 6C). The leadframe strip 100 is then subjected to an etching process to create the contact pads 203, power or ground ring attachment 204 and die attach pad 202 (Figure 6D). The ring 204 can be either a power or a ground ring 204.

One feature of the present invention is the deliberate deposition of the photoresist mask 102 in only a very thin layer (e.g. 2 mils) such that each contact pad 203 is plated up into a columnar shape as it flows over the photoresist mask, resulting in a "mushroom cap" or rivet shape (Figures 6D and 6F). The shape of the contact pads 203 is such that they are capable of being locked into the mold body thereby providing superior board mount reliability. It is also contemplated that a "funnel"

shape may be provided for the contact pads 203 by incorporating an angle on the photoresist mask.

As shown in Figure 6D, several deposition and etching options are available. According to options A-1 and A-2, a layer of flash Cu (50 microinches) is provided over the Cu substrate for creating an etch down cavity following post etching (discussed in greater detail below with reference to Figure 6F) for attaching solder balls (also discussed below with reference to Figure 6G). An etch barrier layer of Au (20 microinches) is then deposited, followed by layers of Ni (40 microinches), and Cu (3-4 mils). According to option A-1, final layers of Ni (40 microinches) and Au (20 microinches) are deposited whereas in Option A-2 a final layer of Ag is deposited (100 – 300 microinches).

In plating Options B-1 and B-2, the initial flash Cu deposition is omitted, and in Options C-1 and C-2 the etch barrier of Au and subsequent Ni deposition are replaced by an etch barrier of tin (100 – 300 microinches).

A singulated semiconductor die 206 is conventionally mounted via epoxy (or other means) to the die attach pad 202, and the epoxy is cured. Gold wires 205 are then bonded between the semiconductor die 206 and peripheral leads or contacts 203. The leadframe 100 is then molded using a modified mold with the bottom cavity being a flat plate, and subsequently cured, as discussed in Applicants' application serial no. 09/095,803. The leadframe 100 after the foregoing steps is as shown in Figure 6E, which includes overmold 401 of cured plastic or epoxy (0.8 mm).

The leadframe 100 is then subjected to a final alkaline etching via full immersion (Figure 6F) which exposes an array or perimeter pattern of exposed contact pads 203, power/ground ring 204 and the die attach pad 206. According to Option A,

an etch down cavity 203B is left after etching away the flash Cu, for attachment of solder balls 203A to contact pads 203, as shown in Figure 6G. At this stage of manufacture, the power/ground ring 204 and die attach pad 202 (which also functions as a ground plane) are fully isolated and exposed. Singulation of the individual units from the full leadframe array strip 100 may then be performed either by saw singulation or die punching resulting in the final configuration of Figure 6H. Since the entire LPCC contains short circuit connections prior to singulation, it is contemplated that the multiple circuits may be gang tested before singulation.

The fabrication process of the present invention may alternatively omit the solder ball attachment step, as shown in Options B and C.

Figure 7 is a bottom plan view of the assembled IC package according to the present invention, with a single row of I/O contacts, while Figures 8A and 8B show array type packages manufactured in accordance with the process of Figures 6A – 6H. In Figure 8A, the contact pads 203 are round, whereas in Figure 8B the contact pads are rectangular. The power/ground ring 204 and the interlocking pattern of the die attach pad/ground plane 202, are clearly shown.

Figure 9 is a bottom plan view according to yet another embodiment of the present invention, with three rows of contact pads 203, and a pair of concentric rings 204. In the present embodiment, one of the rings 204 is a power ring and the other is a ground ring.

Other embodiments of the invention are possible. For example, the two rings may be present, one being a power ring and the other being a ground ring. All such embodiments are believed to be within the sphere and scope of the invention as set forth in the claims appended hereto.